

Low Voltage, Dual DPDT and Quad SPDT Analog Switches

FEATURES

- Low Voltage Operation (1.8 V to 5.5 V)
- Low On Resistance
 - $r_{DS(on)}$: 6 Ω @ 2.7 V
- Low Voltage Logic Compatible
 - DG2019: $V_{INH} = 1$ V
- High Bandwidth: 150 MHz
- QFN-16 Package

BENEFITS

- Ideal for Both Analog and Digital Signal Switching
- Reduced Power Consumption
- High Accuracy
- Reduced PCB Space
- Fast Switching
- Low Leakage

APPLICATIONS

- Cellular Phones
- Audio and Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems
- Portable Instrumentation

DESCRIPTION

The DG2018 and DG2019 are low voltage, single supply analog switches. The DG2018 is a dual double-pole/double-throw (DPDT) with two control inputs that each controls a pair of single-pole/double-throw (SPDT). The DG2019 uses one control pin to operate four independent SPDT switches.

When operated on a +3-V supply, the DG2018's control pins are compatible with 1.8-V digital logic. The DG2019 has an available feature of a V_L pin that allows a 1.0-V threshold for the control pin when V_L is powered with 1.5 V.

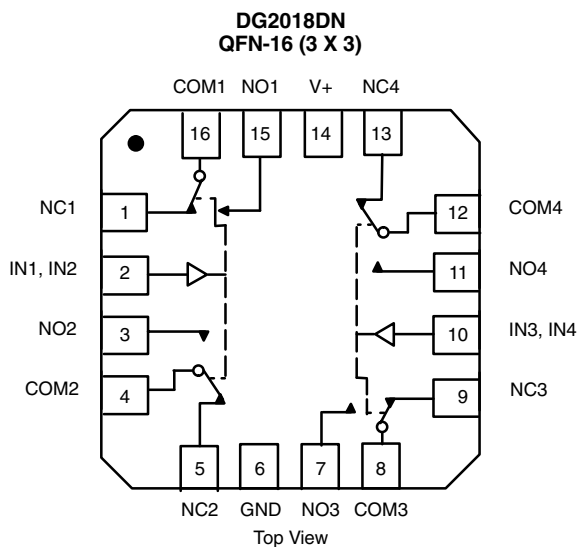
Built on Vishay Siliconix's low voltage submicron CMOS process, the DG2018 and DG2019 are ideal for high

performance switching of analog signals; providing low on-resistance (6 Ω @ +2.7 V), fast speed (T_{on} , T_{off} @ 42 ns and 16 ns), and a bandwidth that exceeds 150 MHz.

The DG2018 and DG2019 were designed to offer solutions that extend beyond audio/video functions, to providing the performance required for today's demanding mixed-signal switching in portable applications.

An epitaxial layer prevents latch-up. Brake-before-make is guaranteed for all SPDT's. All switches conduct equally well in both directions when on, and blocks up to the power supply level when off.

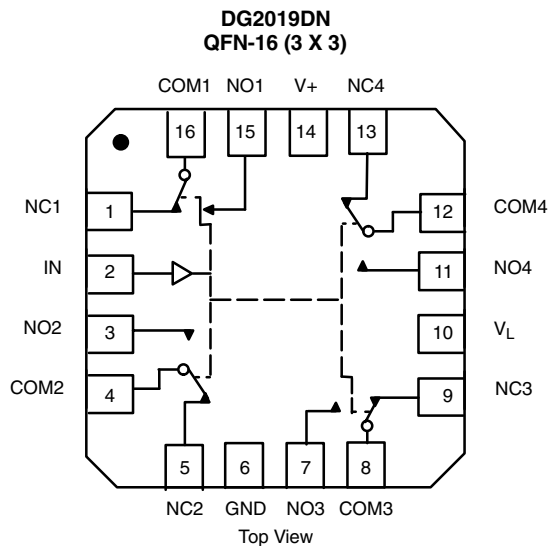
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE		
IN1, IN2		
Logic	NC1 and NC2	NO1 and NO2
0	ON	OFF
1	OFF	ON
IN3, IN4		
Logic	NC3 and NC4	NO3 and NO4
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
Temp Range	Package	Part Number
-40 to 85°C	QFN-16 (3 x 3 mm)	DG2018DN-T1-E4

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE		
Logic	NC1, 2, 3, and 4	NO1, 2, 3, and 4
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
Temp Range	Package	Part Number
-40 to 85°C	QFN-16 (3 x 3 mm)	DG2019DN-T1-E4

ABSOLUTE MAXIMUM RATINGS

Reference to GND	
V+	-0.3 to +6 V
IN, COM, NC, NO	-0.3 to (V+ + 0.3 V)
Continuous Current (Any terminal)	±50 mA
Peak Current (Pulsed at 1 ms, 10% duty cycle)	±100 mA
Storage Temperature (D Suffix)	-65 to 150°C

Power Dissipation (Packages) ^b	
QFN-16 (3 x 3 mm) ^c	850 mW

- Notes:
- a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
 - b. All leads welded or soldered to PC Board.
 - c. Derate 4.0 mW/°C above 70°C



SPECIFICATIONS (V+ = 3 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10% (DG2018 Only) VIN = 0.5 or 1.4 V ^e (DG2019 Only) VL = 1.5 V, VIN = 0.4 or 1.0 V ^e	Temp ^a	Limits −40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} , V _{COM}		Full	0		V+	V
On-Resistance	r _{ON}	V+ = 2.7 V, V _{COM} = 0.2 V/1.5 V I _{NO} , I _{NC} = 10 mA	Room Full		6	12 15	Ω
r _{ON} Flatness	r _{ON} Flatness	V+ = 2.7 V V _{COM} = 0 to V+, I _{NO} , I _{NC} = 10 mA	Room		0.5	2	
r _{ON} Match Between Channels	Δr _{ON}		Room		0.6	3	
Switch Off Leakage Current	I _{NO(off)} , I _{NC(off)}	V+ = 3.3 V, V _{NO} , V _{NC} = 0.3 V/3 V V _{COM} = 3 V/ 0.3 V	Room Full	−1 −10	0.3	1 10	nA
	I _{COM(off)}		Room Full	−1 −10	0.3	1 10	
Channel-On Leakage Current	I _{COM(on)}	V+ = 3.3 V, V _{NO} , V _{NC} = V _{COM} = 0.3 V/ 3 V	Room Full	−1 1.0	0.3	1 10	
Digital Control							
Input High Voltage	VINH		DG2018	Full	1.4		V
		VL = 1.5 V	DG2019	Full	1.0		
Input Low Voltage	VINL		DG2018	Full		0.5	
		VL = 1.5 V	DG2019	Full		0.4	
Input Capacitance	Cin	f = 1 MHz	Full		9		pF
Input Current	I _{INL} or I _{INH}	VIN = 0 or V+	Full	−1		1	μA
Dynamic Characteristics							
Turn-On Time	t _{ON}	V _{NO} or V _{NC} = 2.0 V, RL = 300 Ω, CL = 35 pF	Room Full		42	55 65	ns
Turn-Off Time	t _{OFF}		Room Full		16	25 35	
Break-Before-Make Time	t _d	V _{NO} or V _{NC} = 2.0 V, RL = 50 Ω, CL = 35 pF	Full	1			
Charge Injection ^d	Q _{INJ}	CL = 1 nF, V _{GEN} = 0 V, R _{GEN} = 0 Ω	Room		−1.46		pC
Off-Isolation ^d	OIRR	RL = 50 Ω, CL = 5 pF, f = 1 MHz	Room		−54		dB
Crosstalk ^d	X _{TALK}		Room		−53		
NO, NC Off Capacitance ^d	C _{NO(off)}	VIN = 0 or V+, f = 1 MHz	Room		9		pF
	C _{NC(off)}		Room		9		
Channel-On Capacitance ^d	C _{NO(on)}		Room		30		
	C _{NC(on)}		Room		30		
Power Supply							
Power Supply Current	I+	VIN = 0 or V+	Full		0.01	1.0	μA

Notes:

- Room = 25°C, Full = as determined by the operating suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- Guarantee by design, nor subjected to production test.
- V_{IN} = input voltage to perform proper function.

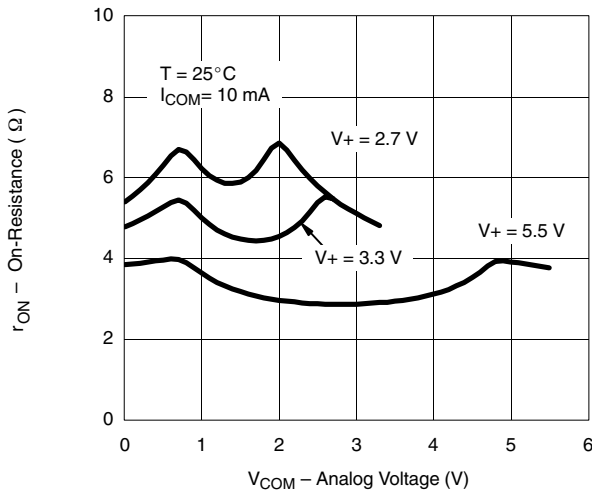
SPECIFICATIONS (V+ = 5 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ±10%, (DG2018 Only) VIN = 0.8 or 1.8 V ^e (DG2019 Only) VL = 1.5 V, VIN = 0.4 or 1.0 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} , V _{COM}		Full	0		V+	V
On-Resistance	r _{ON}	V+ = 4.5 V, V _{COM} = 3 V, I _{NO} , I _{NC} = 10 mA	Room Full		4	8 10	Ω
r _{ON} Flatness	r _{ON} Flatness	V+ = 4.5 V V _{COM} = 0 to V+, I _{NO} , I _{NC} = 10 mA	Room		0.6	1.2	
r _{ON} Match Between Channels	Δr _{ON}		Room		0.6	1.2	
Switch Off Leakage Current ^f	I _{NO(off)} , I _{NC(off)}	V+ = 5.5 V V _{NO} , V _{NC} = 1 V/4.5 V, V _{COM} = 4.5 V/1 V	Room Full	-1 -10	0.03	1 10	nA
	I _{COM(off)}		Room Full	-1 -10	0.03	1 10	
Channel-On Leakage Current ^f	I _{COM(on)}	V+ = 5.5 V, V _{NO} , V _{NC} = V _{COM} = 1 V/4.5 V	Room Full	-1 -10	0.03	1 10	
Digital Control							
Input High Voltage	VINH		DG2018	Full	1.8		V
		VL = 1.5 V	DG2019	Full	1.0		
Input Low Voltage	VINL		DG2018	Full		0.8	
		VL = 1.5 V	DG2019	Full		0.4	
Input Capacitance	Cin		Full		9		pF
Input Current	I _{INL} or I _{INH}	VIN = 0 or V+	Full	1		1	μA
Dynamic Characteristics							
Turn-On Time	t _{ON}	V _{NO} or V _{NC} = 3 V, RL = 300 Ω, CL = 35 pF	Room Full		44	48 52	ns
Turn-Off Time	t _{OFF}		Room Full		19	33 35	
Break-Before-Make Time	td	V _{NO} or V _{NC} = 3 V, RL = 50 Ω, CL = 35 pF	Full	1			
Charge Injection ^d	Q _{INJ}	CL = 1 nF, V _{GEN} = 0 V, R _{GEN} = 0 Ω	Room		-2.46		pC
Off-Isolation ^d	OIRR	RL = 50 Ω, CL = 5 pF, f = 1 MHz	Room		-54		dB
Crosstalk ^d	X _{TALK}		Room		-53		
Source-Off Capacitance ^d	C _{NO(off)}	VIN = 0 or V+, f = 1 MHz	Room		7.5		pF
	C _{NC(off)}		Room		7.5		
Channel-On Capacitance ^d	C _{NO(on)}		Room		30		
	C _{NC(on)}		Room		30		
Power Supply							
Power Supply Range	V+			1.8		5.5	V
Power Supply Current	I+	VIN = 0 or V+	Full		0.01	1.0	μA

Notes:

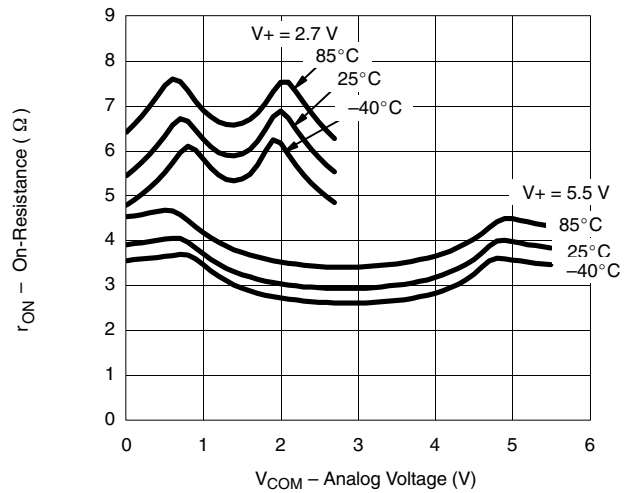
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- V_{IN} = input voltage to perform proper function.
- Not production tested.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

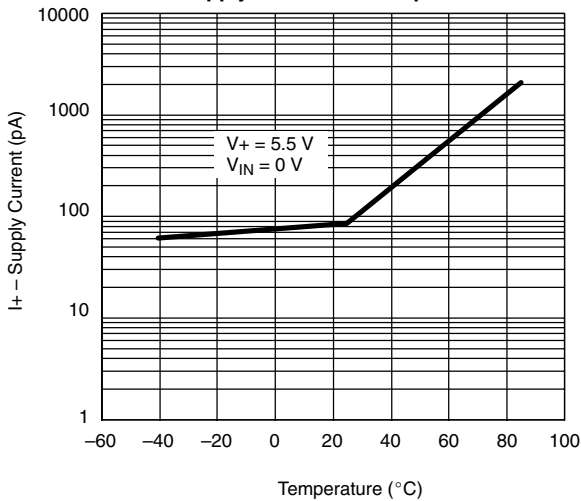
r_{ON} vs. V_{COM} and Supply Voltage



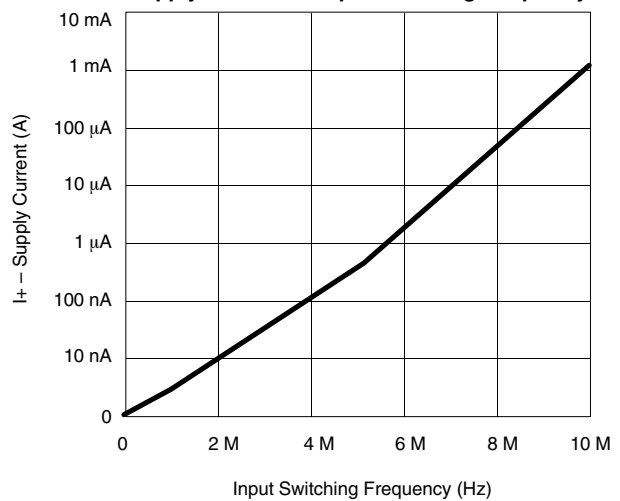
r_{ON} vs. Analog Voltage and Temperature



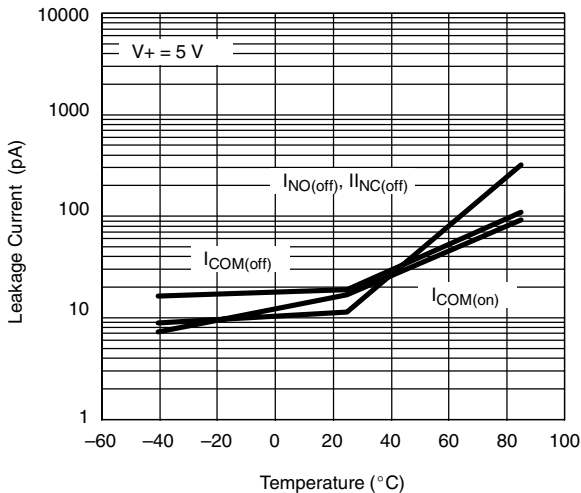
Supply Current vs. Temperature



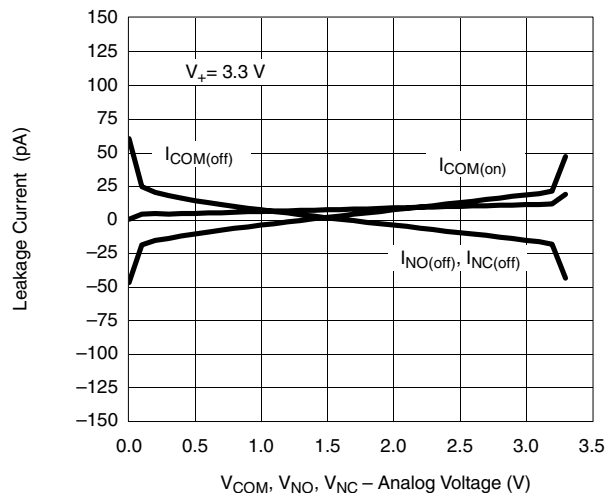
Supply Current vs. Input Switching Frequency



Leakage Current vs. Temperature

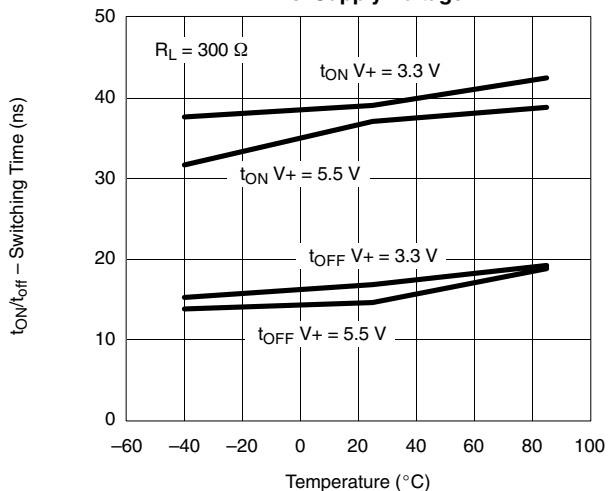


Leakage vs. Analog Voltage

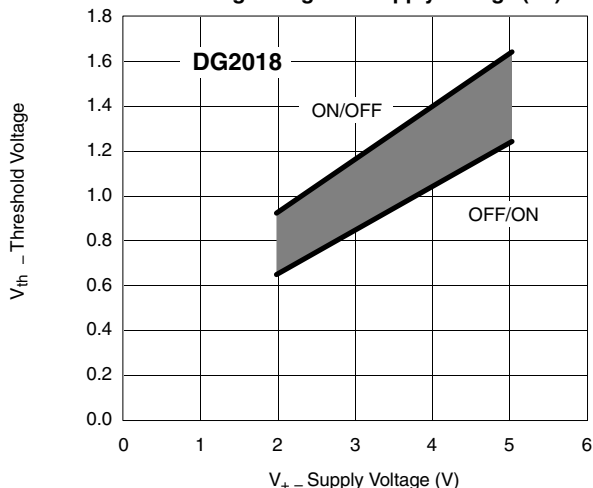


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

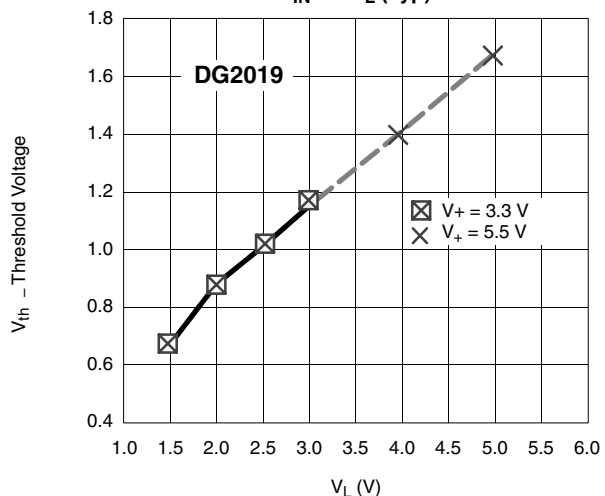
Switching Time vs. Temperature vs. Supply Voltage



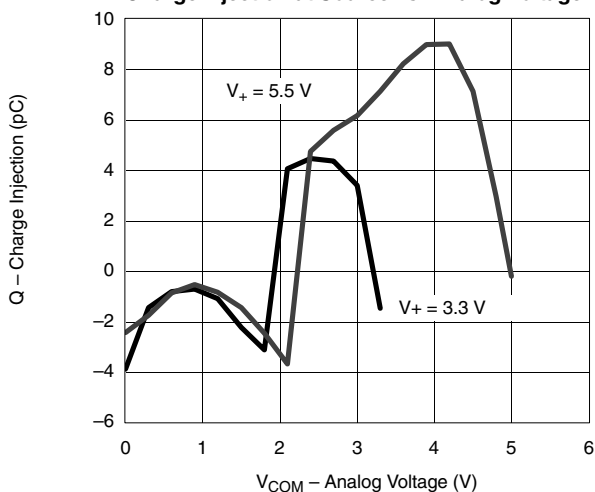
Switching Voltage vs. Supply Voltage (V+)



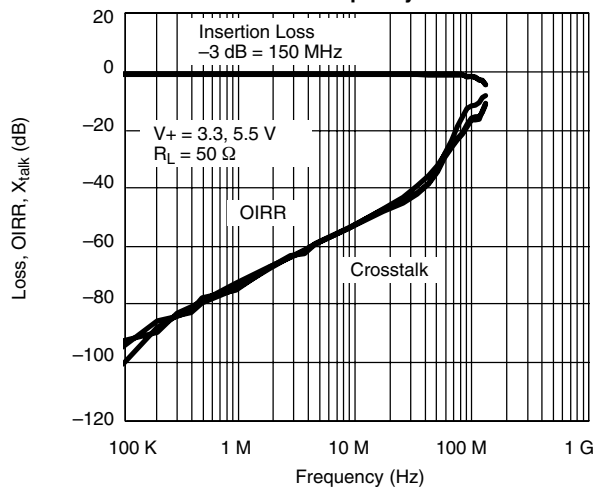
VIN vs. VL (Typ)



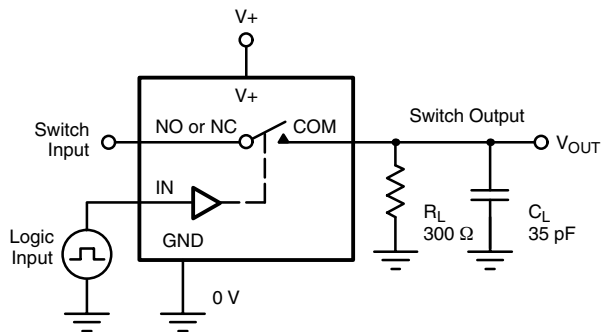
Charge Injection at Source vs. Analog Voltage



Insertion Loss, Off Isolation and Crosstalk vs. Frequency

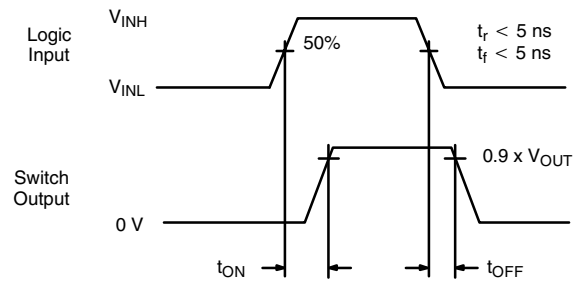


TEST CIRCUITS



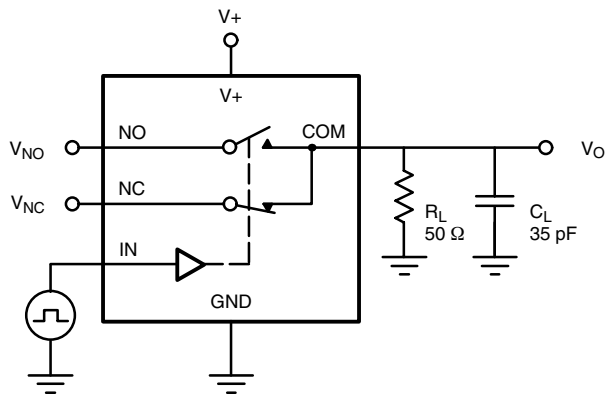
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

FIGURE 1. Switching Time



C_L (includes fixture and stray capacitance)

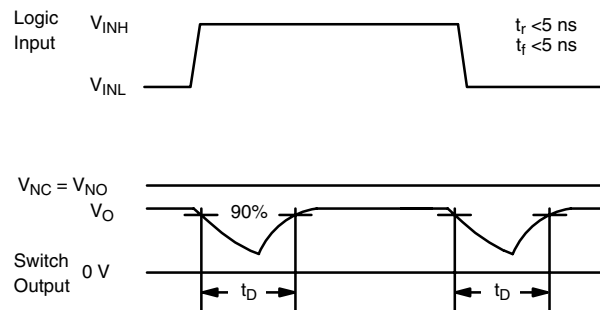
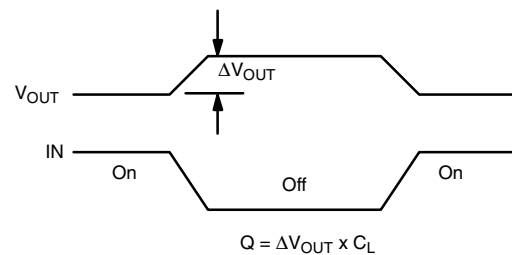
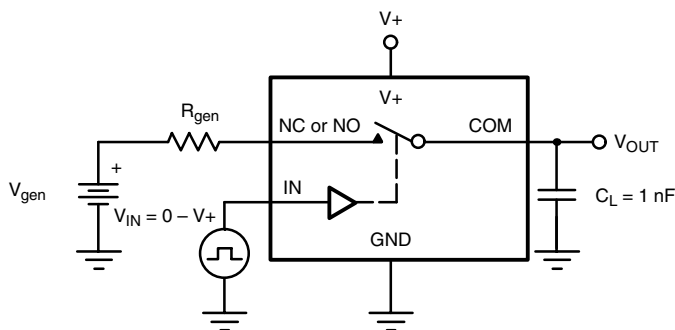


FIGURE 3. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

FIGURE 2. Charge Injection

TEST CIRCUITS

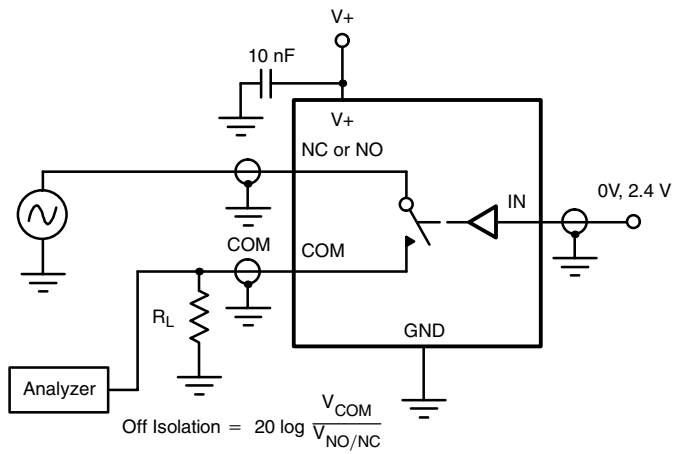


FIGURE 4. Off-Isolation

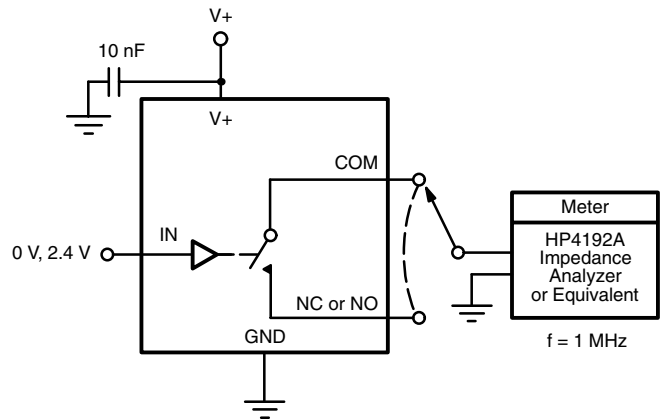


FIGURE 5. Channel Off/On Capacitance



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